John Swindle, Precept Technologies
Roland Scherzinger, Agilent Technologies

CompactPCI: Functional Design Verification of Communication Equipment

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Innovating the HP Way

Agenda

- Motivation to convert to CompactPCI
- Generic features of CompactPCI
- Where CompactPCI fits in the system: PCI architecture
- Verifying cellular base station transmitter/receiver modules
- Conclusion

Motivation to Convert to CompactPCI

- Reduced design time
- Reduced manufacturing cost
- Reduced support cost

- You can and must use PCI!
- You aren't alone!

Analytical tools based on concepts developed by Intel

Generic Features of CompactPCI

- Platform independence; industry-standard bus
- Up to eight cards per bus
- Expandable to 256 buses per system
- Mechanical, electrical and logical specification
- Hot swap capability

Generic Features of CompactPCI

- Low power consumption
- Efficient burst transactions
- Bus speed to 66MHz and bus width to 64-bit
- Concurrency
- Peer-to-peer bus mastering

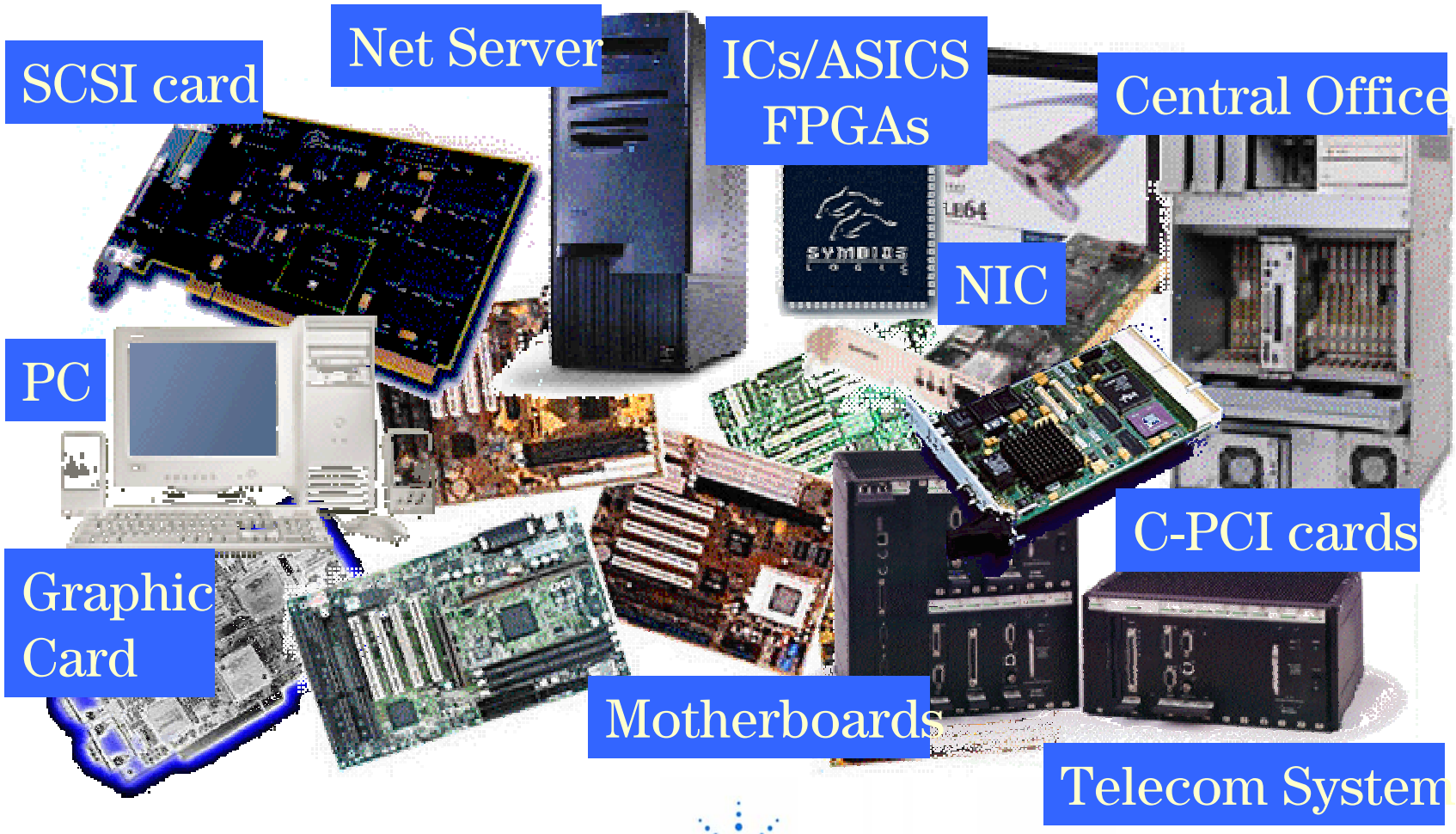
Generic Features of CompactPCI

- Hidden arbitration
- Low pin count
- Parity
- Three address spaces
- Software configurable

Generic Features of CompactPCI

- Industry standard software
- Software transparency for ISA support and legacy IDE support
- User-defined pins
- System Management Bus

Where Is PCI?



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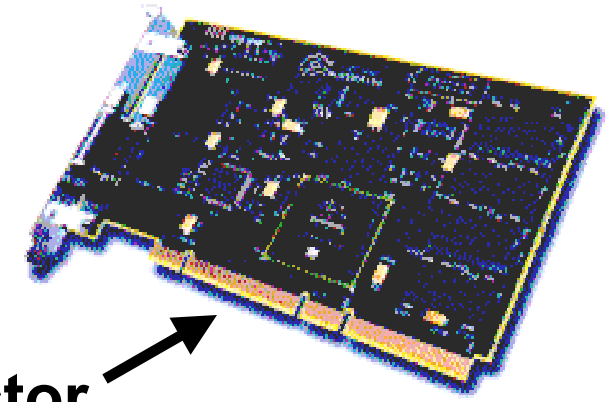
PCI Form Factors

Standard short PCI card

Used as the expansion bus in PCs

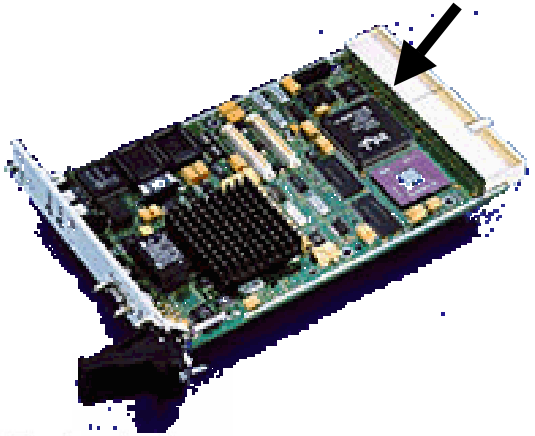
Example: LAN card



CompactPCI form factor

Used in telecom and embedded applications

Example: transmitter/receiver cards



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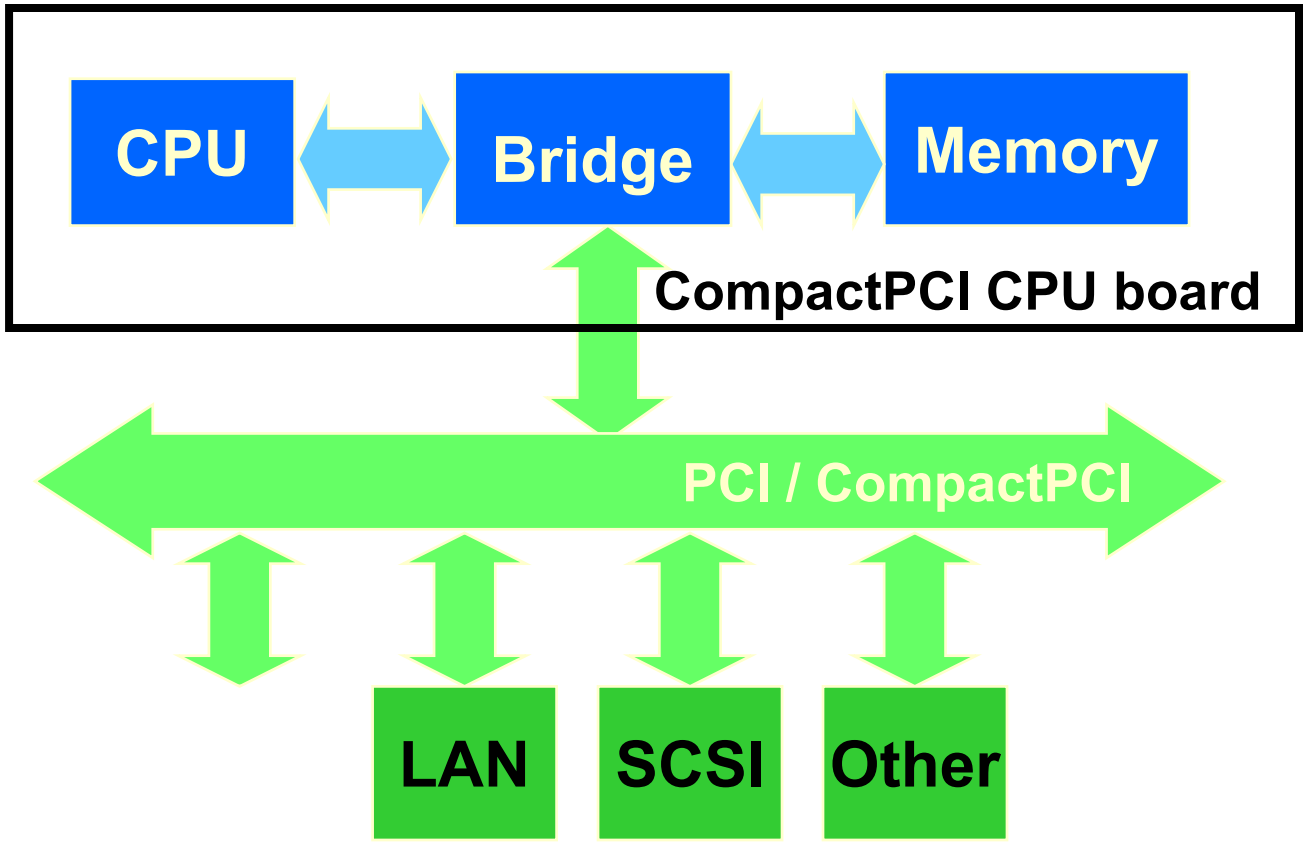
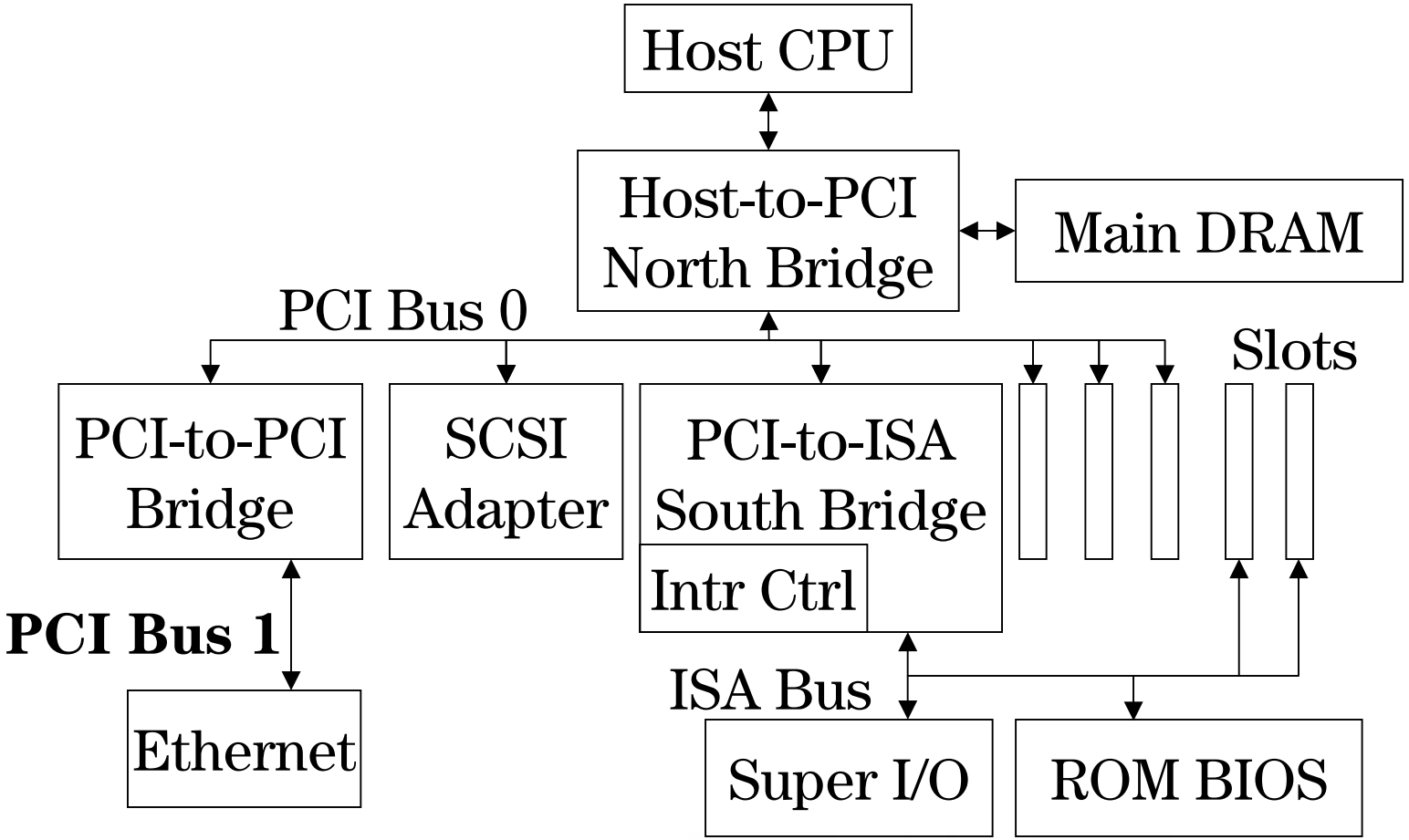
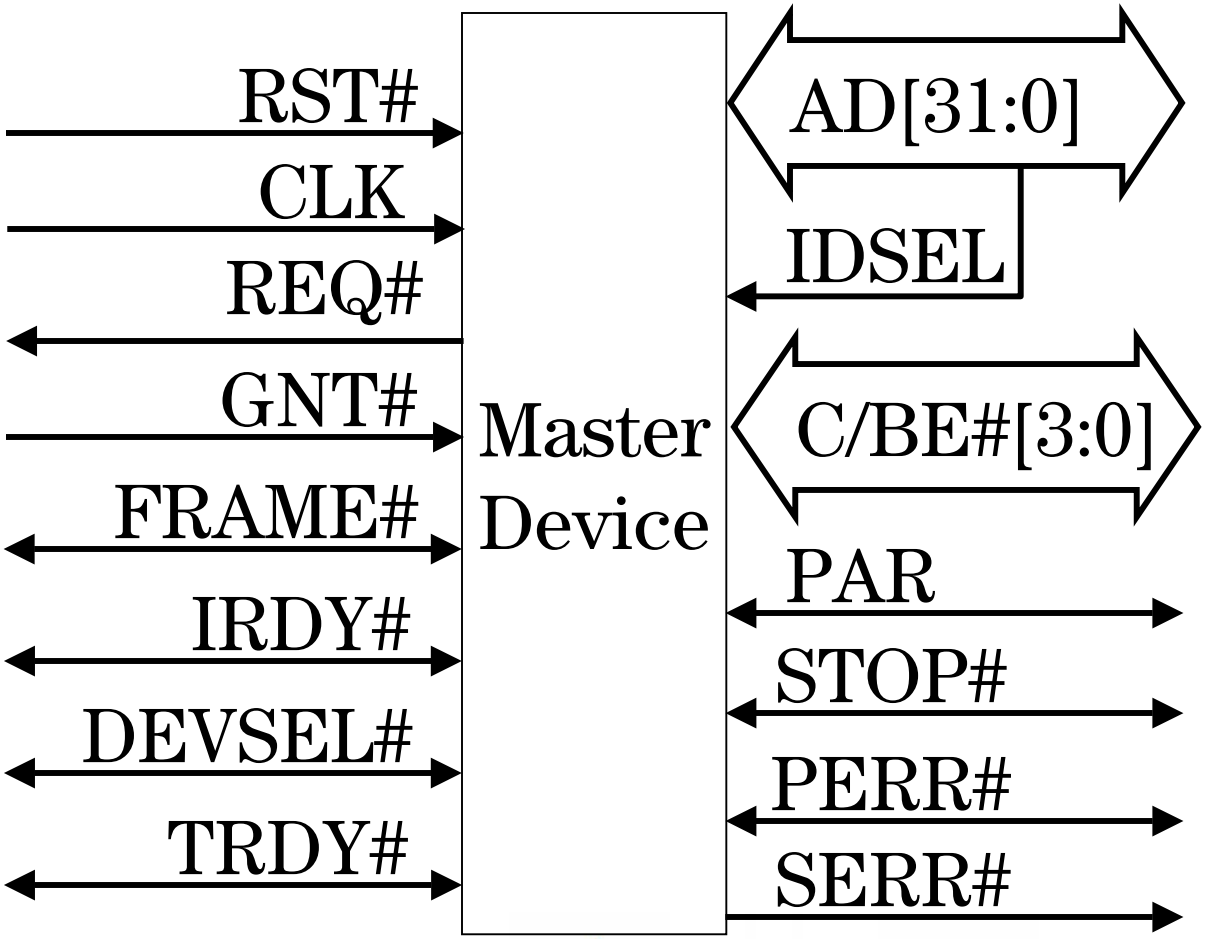
PCI Architecture



PCI Architecture
Multiple PCI Buses



PCI Architecture
49 Required Pins for Master



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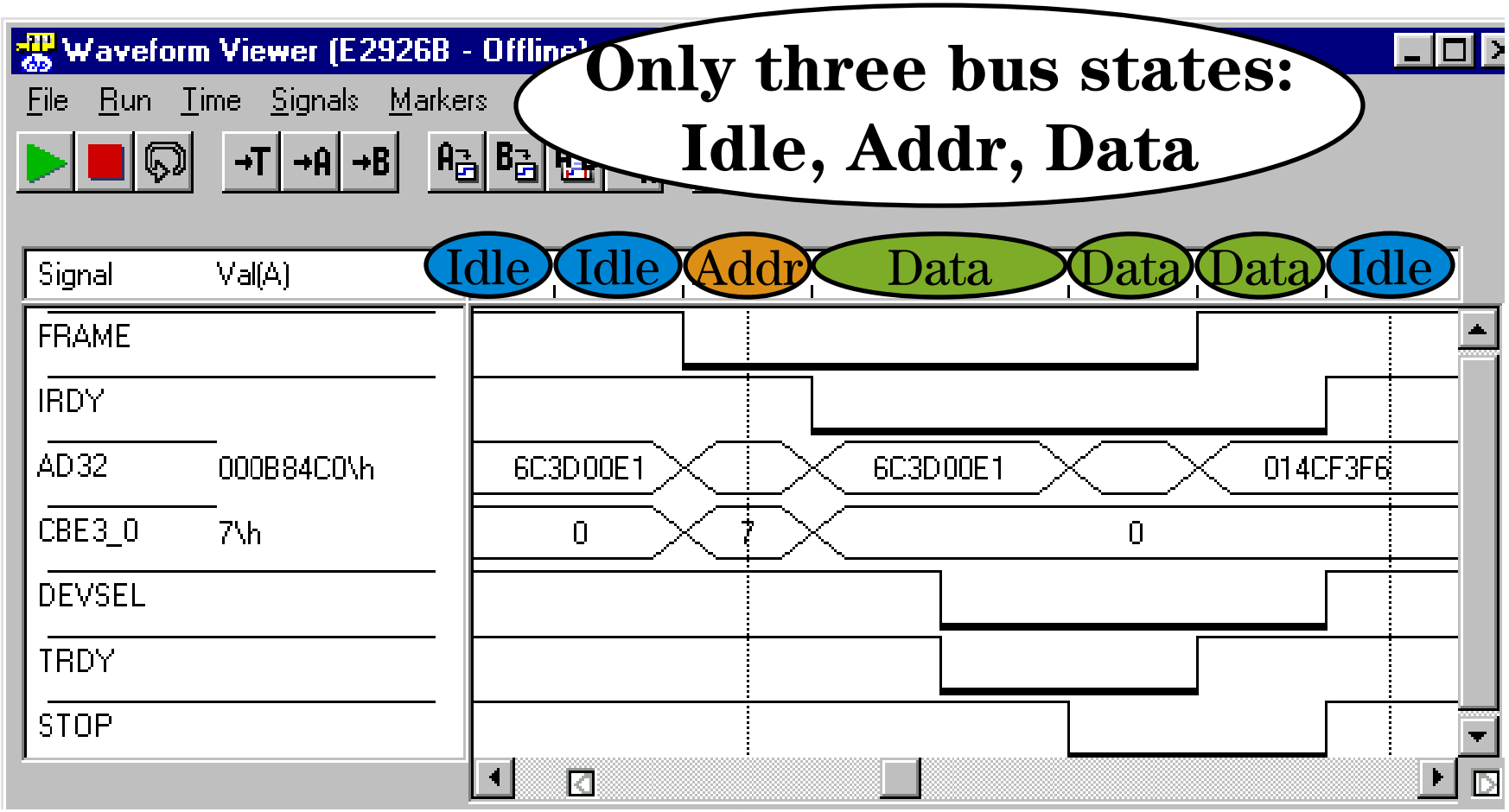
PCI Architecture
Basic Timing



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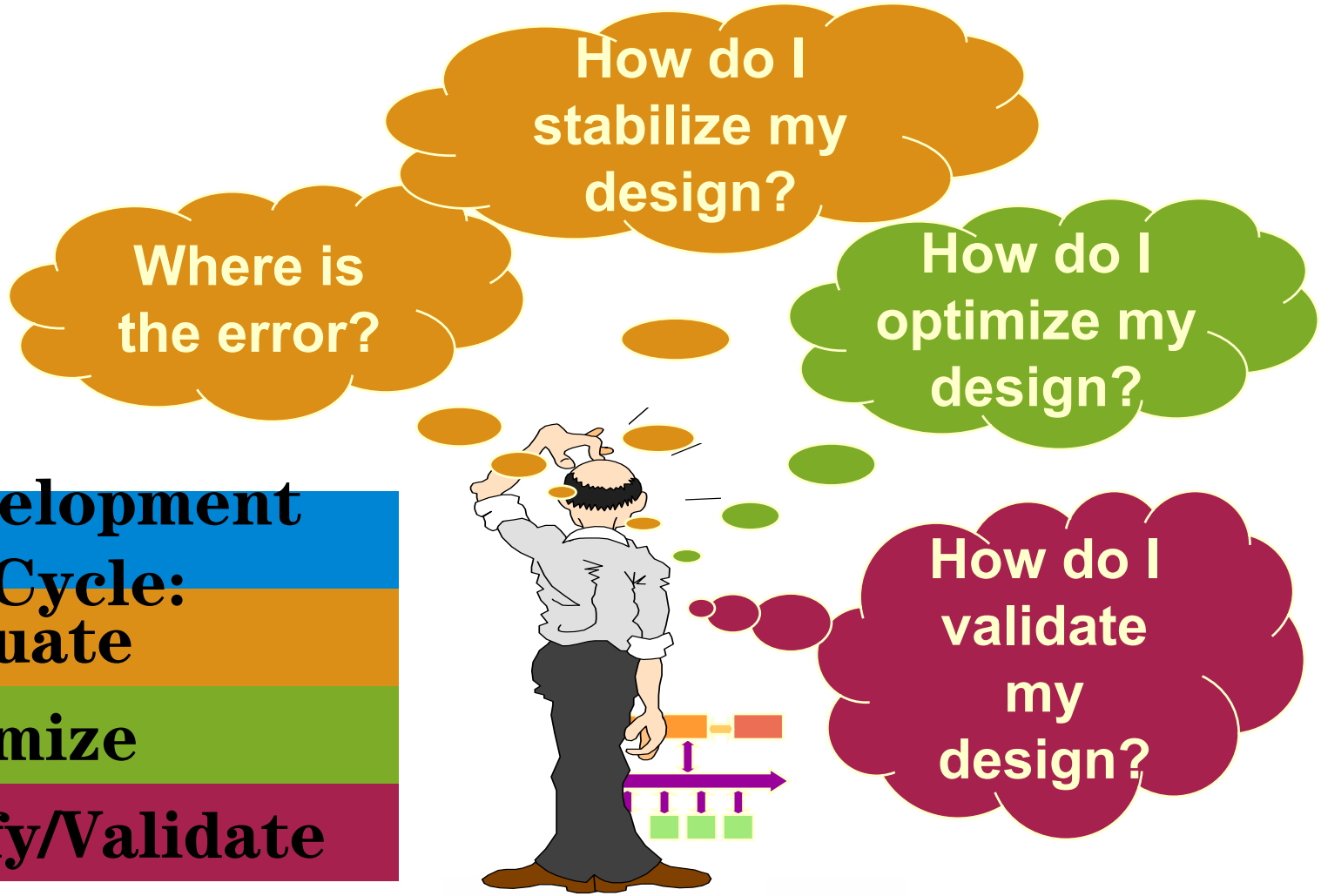
The Typical Problems



Development Cycle:

- **Evaluate**
- **Optimize**
- **Verify/Validate**

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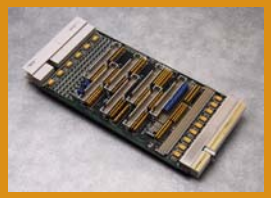
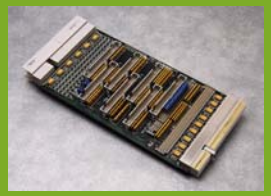
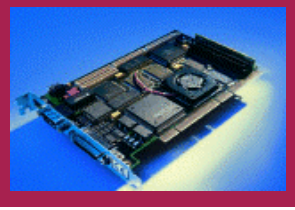
CompactPCI Solution Portfolio
Agilent Technologies and FuturePlus

	16700	FS3020	E2940A
Timing verification			
C-PCI bus analysis			
Compliance test & Design Verification			

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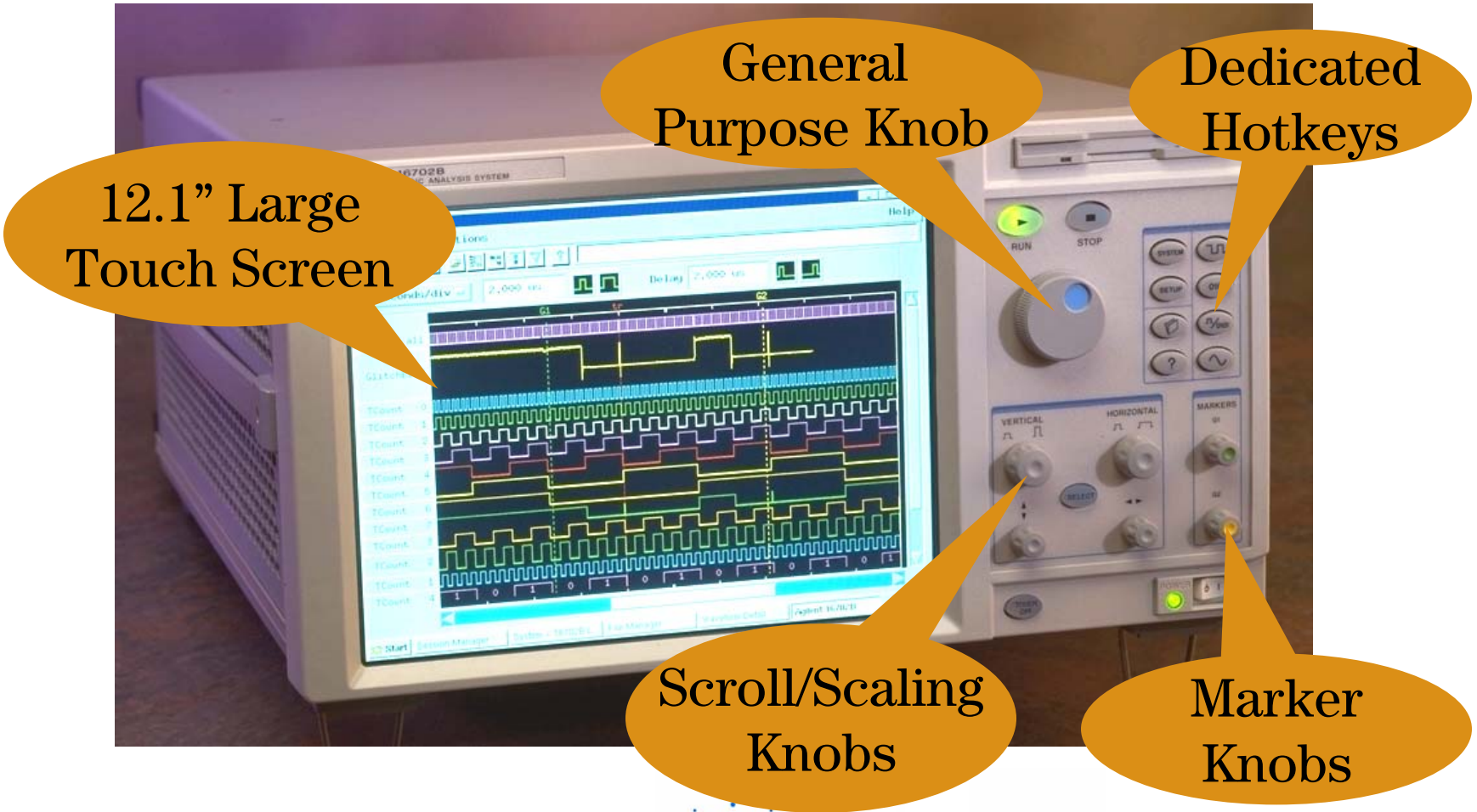
Agilent 16702B Frames



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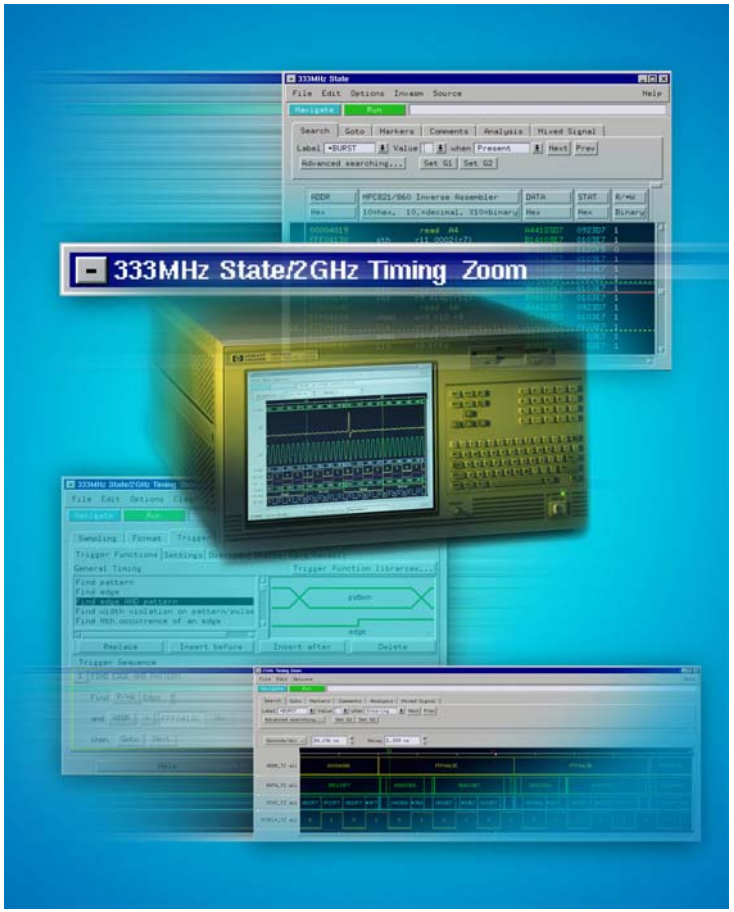
Logic Analysis Modules for 16702B Frames

- Timing analysis to 800/400 MHz
- State analysis to 200 MHz
- 400 MHz “Turbo” State Triggering
- 2 GHz Timing Zoom thru same probe, 16K
- Memory depths to 32M samples
- Up to 340 channels/group



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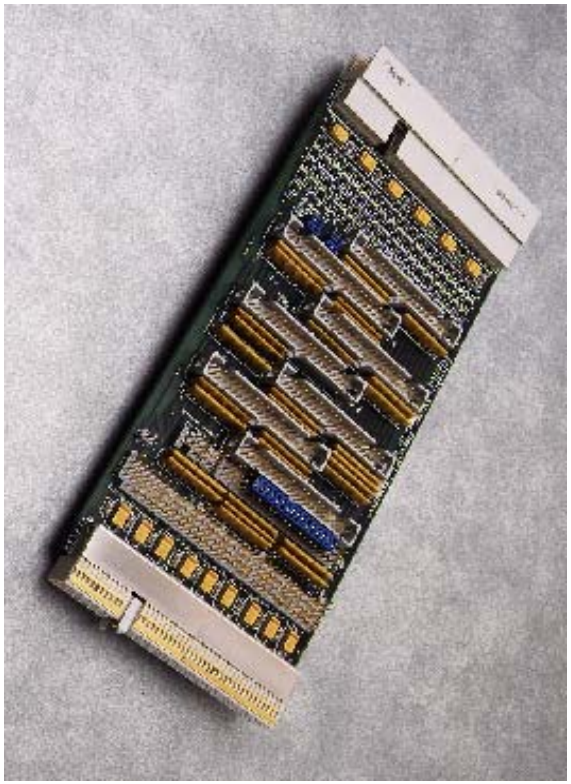
FuturePlus Systems

- Agilent Channel Partner, Premier Level
- Focus on solutions for computer buses
- Provides mechanical and electrical connection from the user's bus to Agilent logic analyzers
- Provides software that configures the logic analyzer and reconstructs bus transactions from acquired data

FuturePlus CompactPCI Bus Probe FS3020

- For 32- or 64-bit CompactPCI Bus up to 33 MHz
- Inverse assembler, state and timing analysis
- Monitors system arbiter
- Requires 4 to 7 logic analyzer pods
- Includes extender function and test points



Also available as Agilent product FSI-60021

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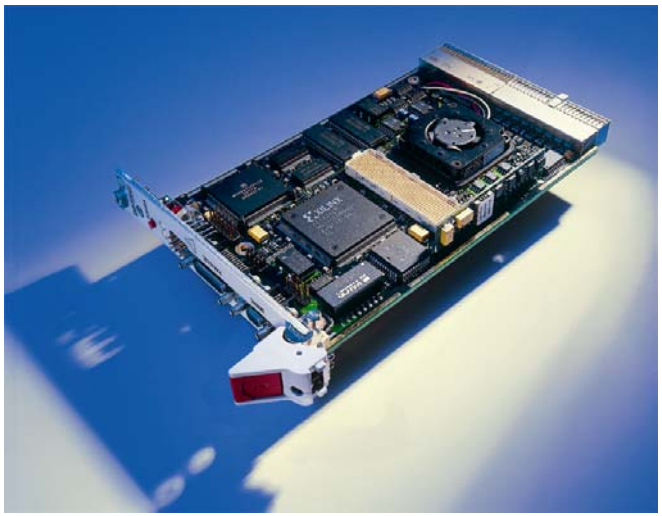
Agilent E2940A Exerciser/Analyzer Key Features

- Single 3U CompactPCI card
- 66 MHz PCI Analyzer / 33 MHz PCI Exerciser, master/target
- Full 32/64-bit PCI data, address and command support
- Supports all PCI signals
- Hot swappable



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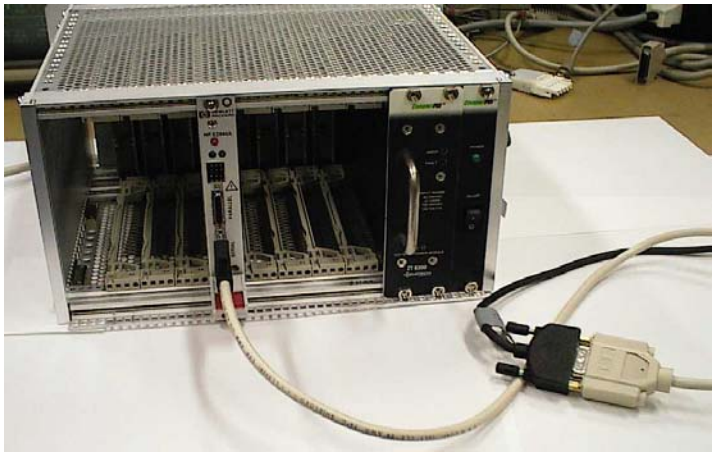
Agilent E2940A Exerciser/Analyzer Key Features

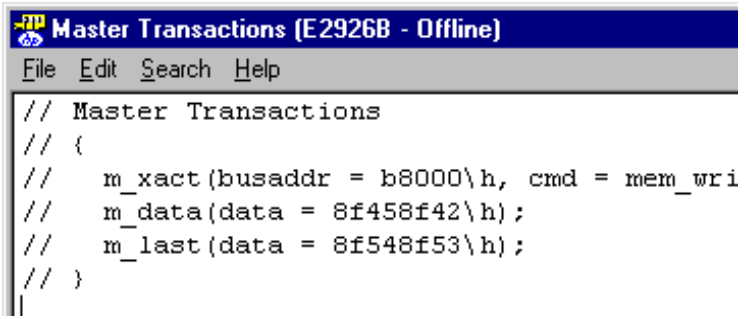
- PCI protocol check and setup and hold timing analysis (250 ps resolution)
- Real-time and statistical analysis of PCI bus performance
- Up to 4M PCI state memory
- Up to 512 KB on-board data memory
- 24 pattern terms and 64-level trigger sequencer

Agilent E2940A Exerciser/Analyzer HW & SW Control

- Control via system-under-test (SUT) host, or
- External control by serial or fast parallel interface for transparency to SUT



- Control via GUI and/or C-API
- Protocol Permutation
- System Verification Pkg



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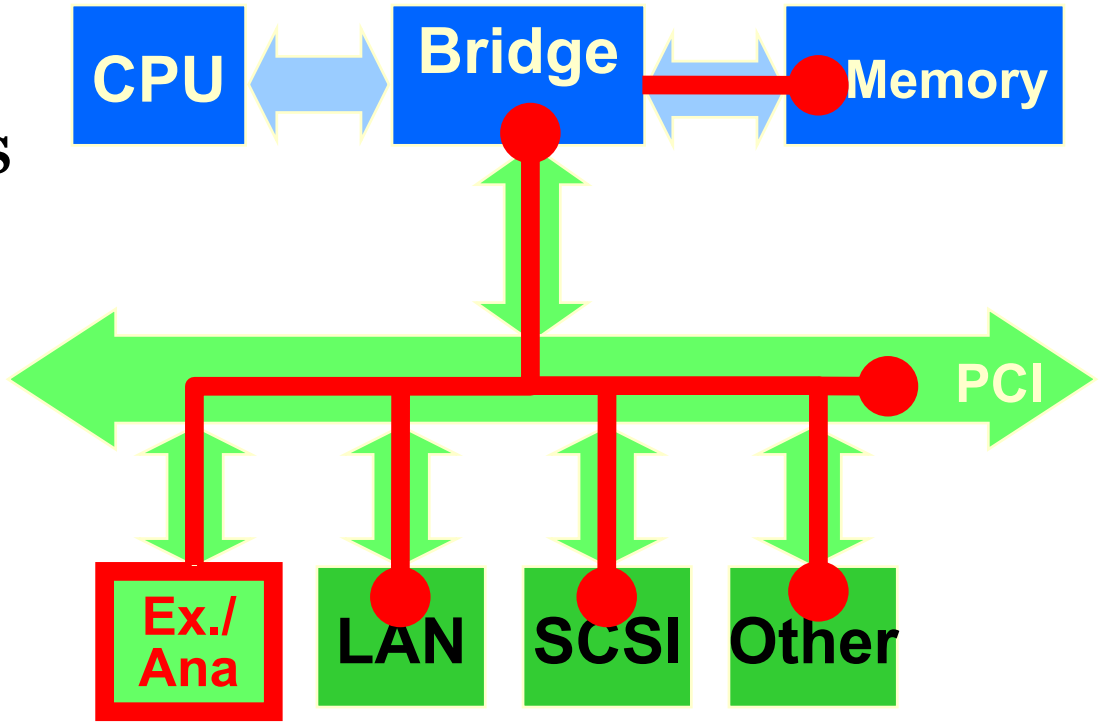
What Does the Agilent E2940A CompactPCI Exerciser / Analyzer Do?

At a central position, it provides an excellent window to:

- Monitor traffic
- Measure performance
- Generate traffic
- Check PCI protocol
- Check PCI timing



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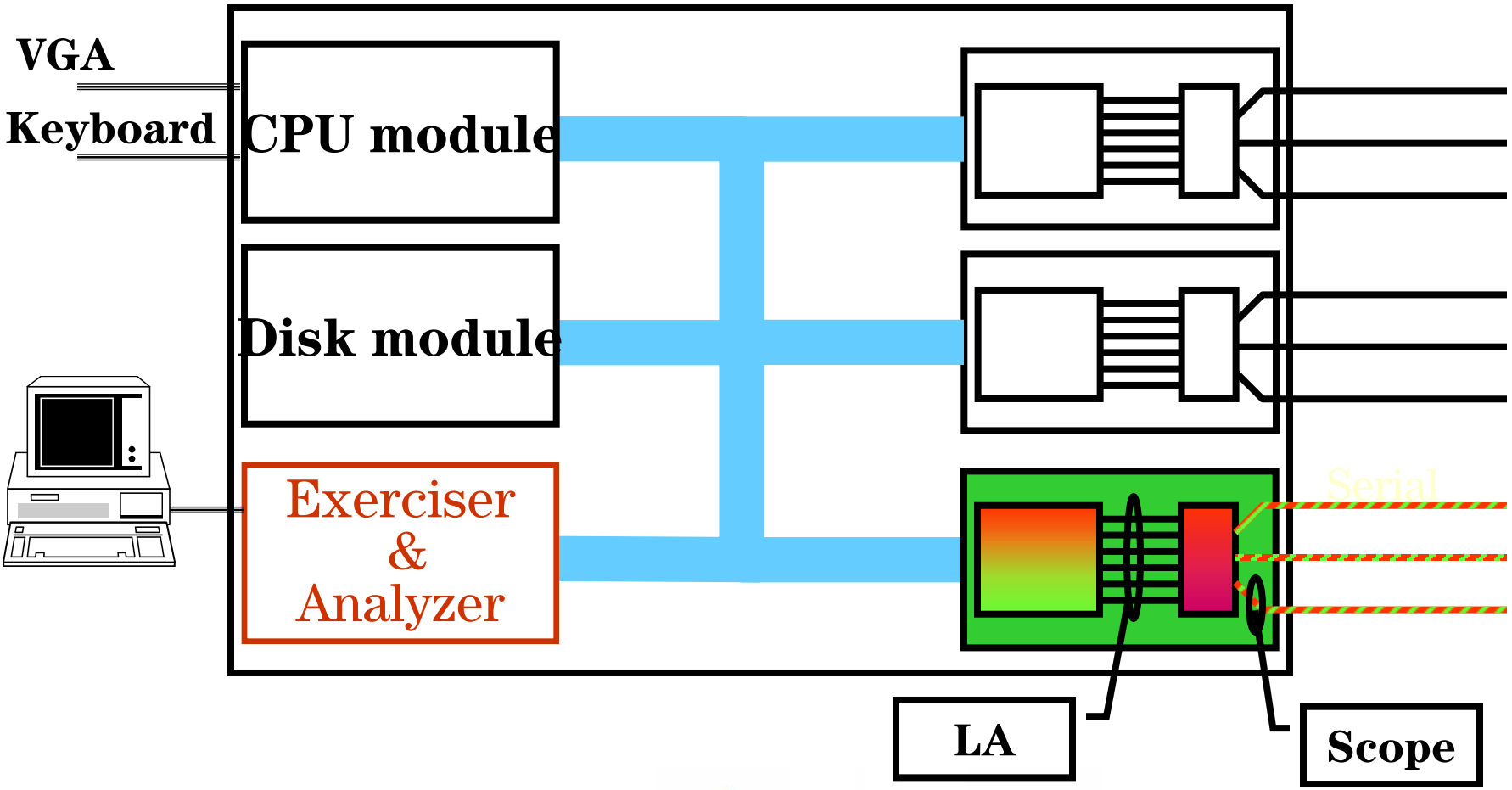
Example: Verify Transmitter/Receiver Modules of a Cellular Base Station



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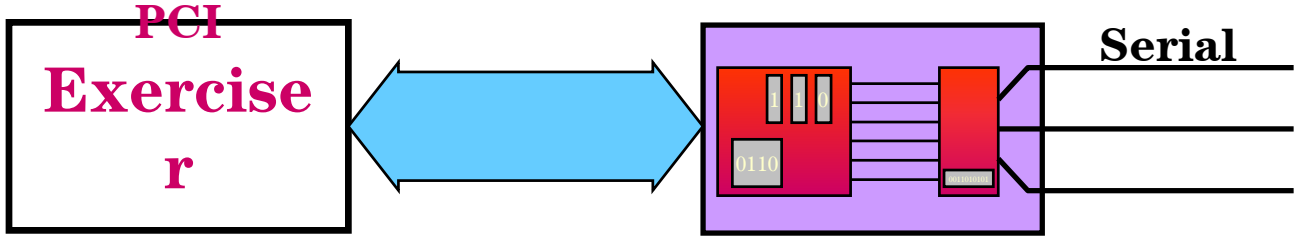
Initial Module Bring-Up



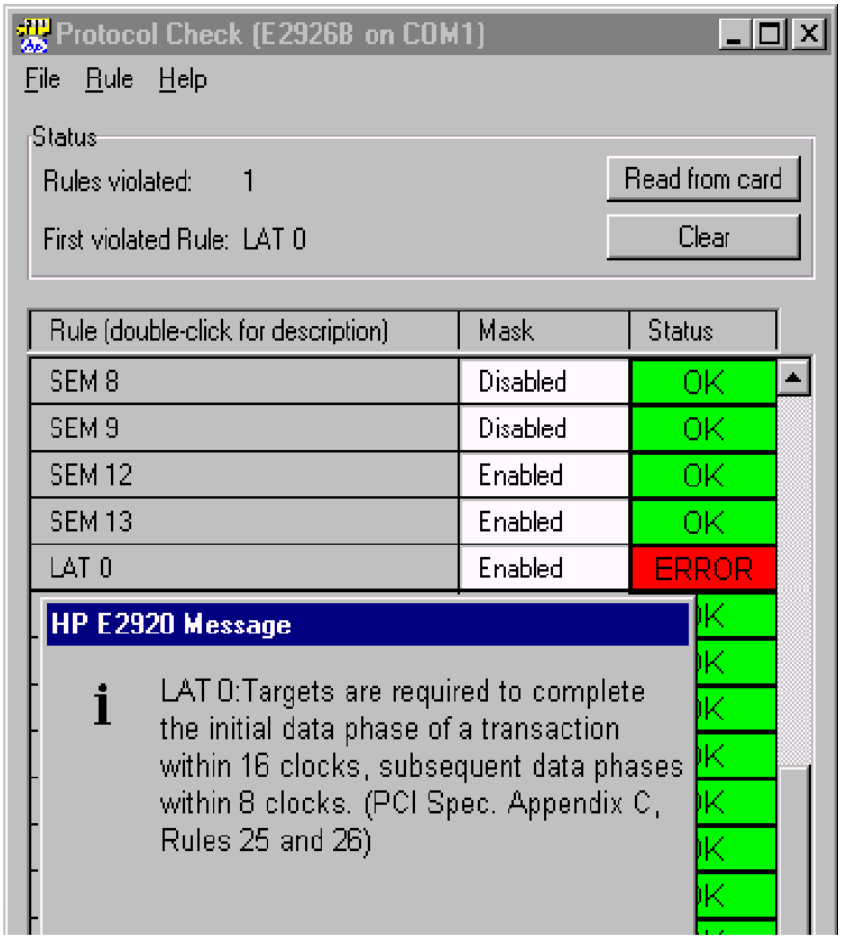
System Monitor:

In the early phase of module bring-up, the master capability of a CompactPCI Exerciser is heavily used to monitor and control the systems/module status.

Initial Module Bring-Up

E2940A checks 53 protocol rules in real time, not sampled and post-processed.

Basic setup and hold timing can also be verified. For more accuracy, use 16700 logic analyzer.



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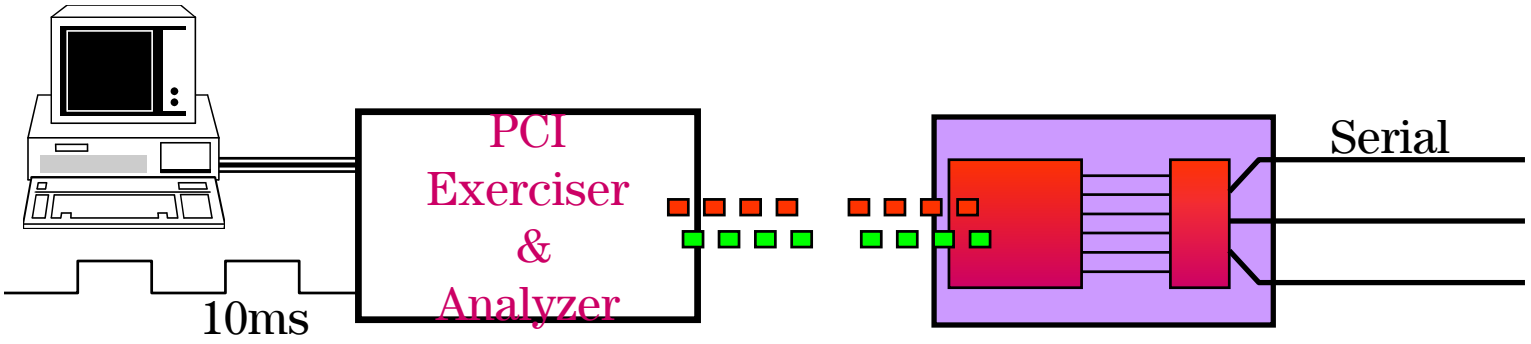
Functional Transmitter Module Test



- Correct handling of data blocks sent to and from the transmitter/receiver module
- Susceptibility to data delays
- Handling of data queues

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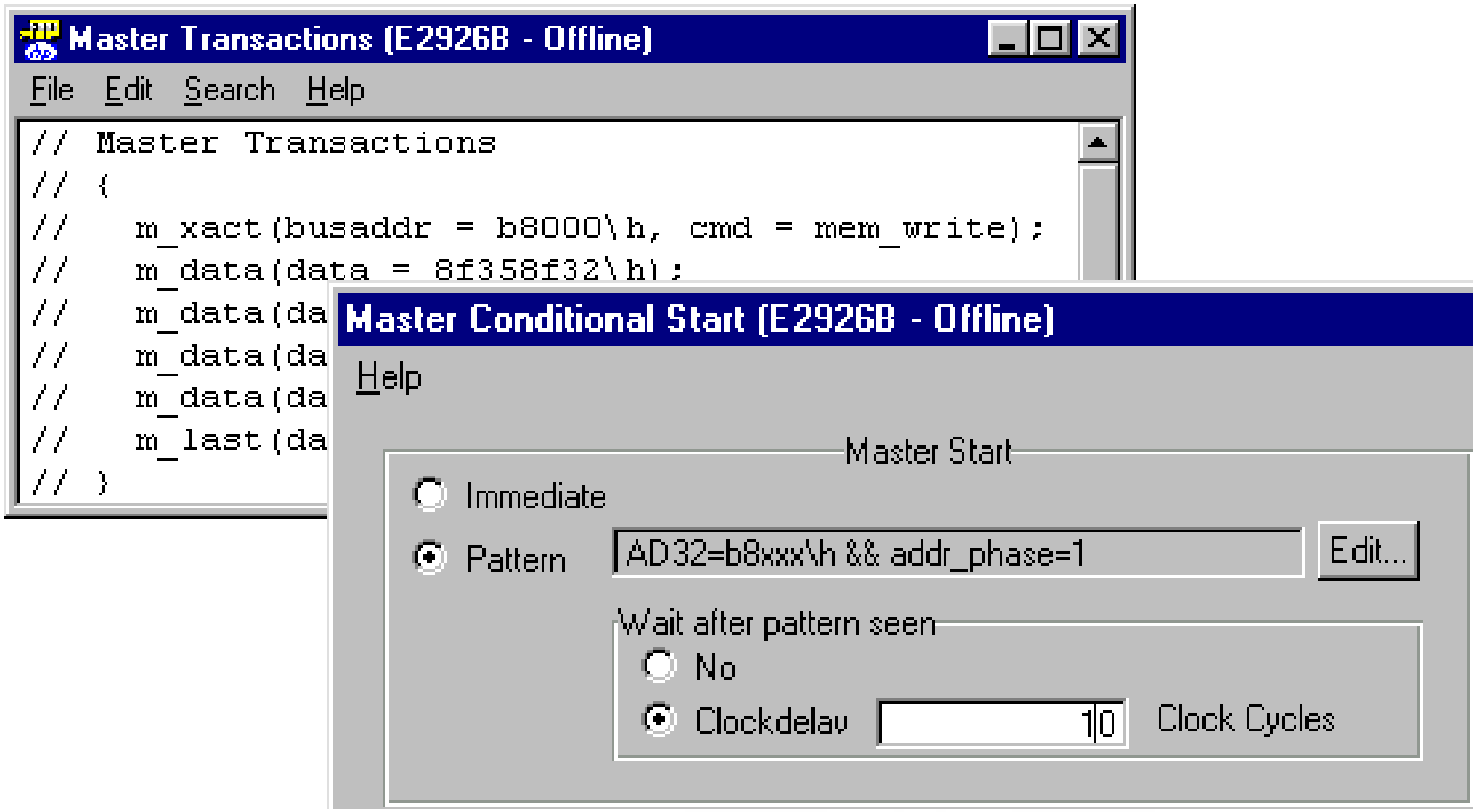
Functional Transmitter Module Test



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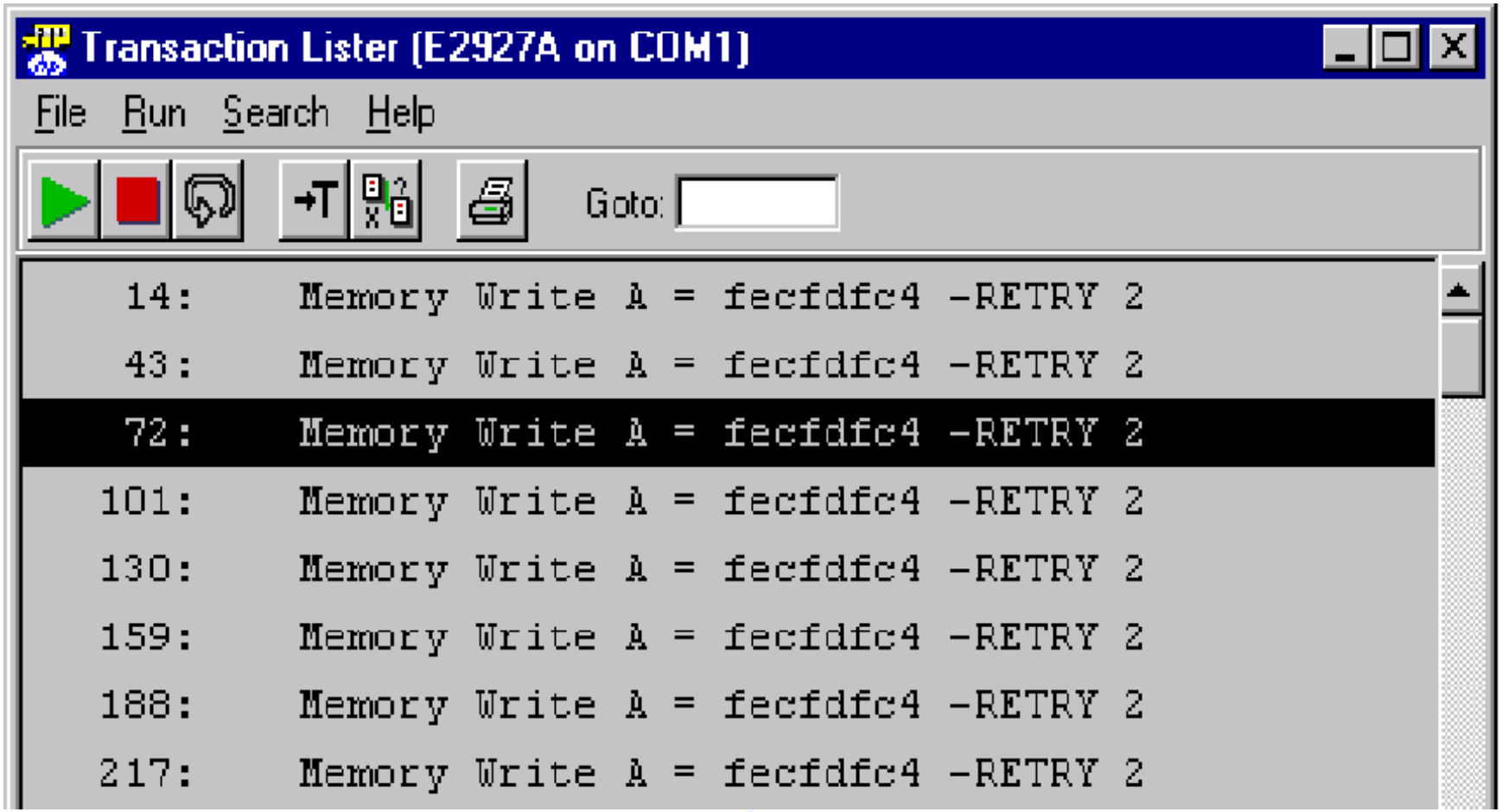
Premature Terminations



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Performance is #1 Concern

Most other problems are solved by the availability of high-quality components, boards and systems from many vendors. The maturity of the specification usually assures hardware interoperability of basic designs.

Performance

A little latency consumes a lot of bandwidth.

Example: 32-bit, 33MHz bus with only three wait states in the entire transaction.

Bytes transferred	Throughput	
16	59 MB/s	<50% of theoretical
64	102 MB/s	
128	115 MB/s	<90%
256	124 MB/s	>90%

Performance

Surprised? What causes performance problems?

- Multiplexing (without split transactions) means no pipelining. Much of the latency is explicitly visible on the bus. PCI is tuned for thruput at the expense of latency.
- Latency rules don't solve the throughput issues.
- Depth of topology, delayed transactions and transaction reordering affect latency.

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Performance

Recommendations for performance:

- Choose agents that have low latency
- Choose agents with deep buffers
- Choose agents which use optimized commands
- Choose bridges with deep buffers and capable of handling multiple delayed transactions
- Measure performance with the Agilent analyzer

Performance

The Analyzer has better visibility and control than other agents on the bus, better than that of the host bridge.

Much of the PCI latency and throughput are transparent to software, that is, not under the control of software or the host processor. Only coarse performance measurements may be performed by the host processor's software.

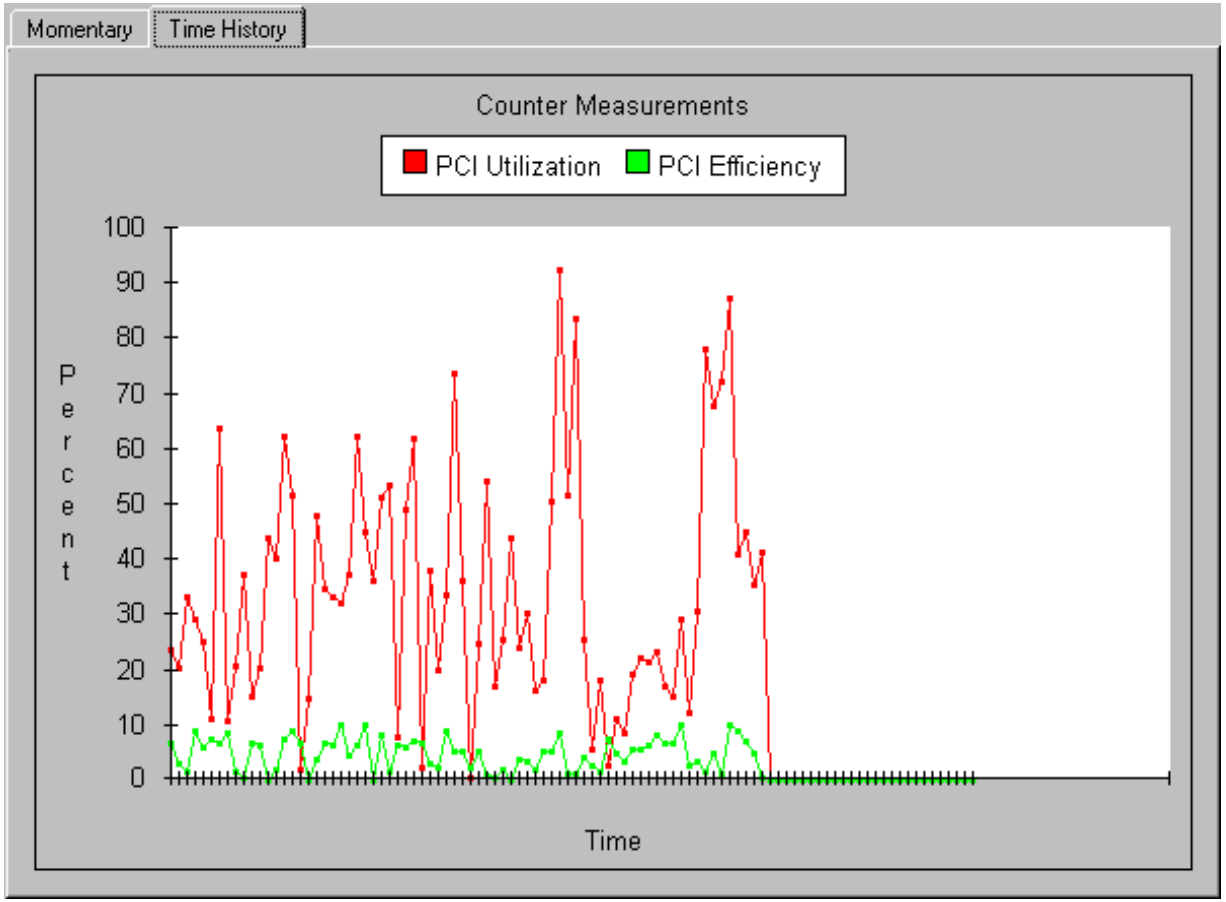
Performance

Analyzer needs to be able to:

- Measure bus utilization
- Measure bus efficiency
- Track delayed transactions
- Track sequences of events (transaction order)
- Exercise the system across many bridges (using multiple Exercisers and Analyzers)

Performance Measurements: Real Time Counter

High utilization and low efficiency indicate a potential problem



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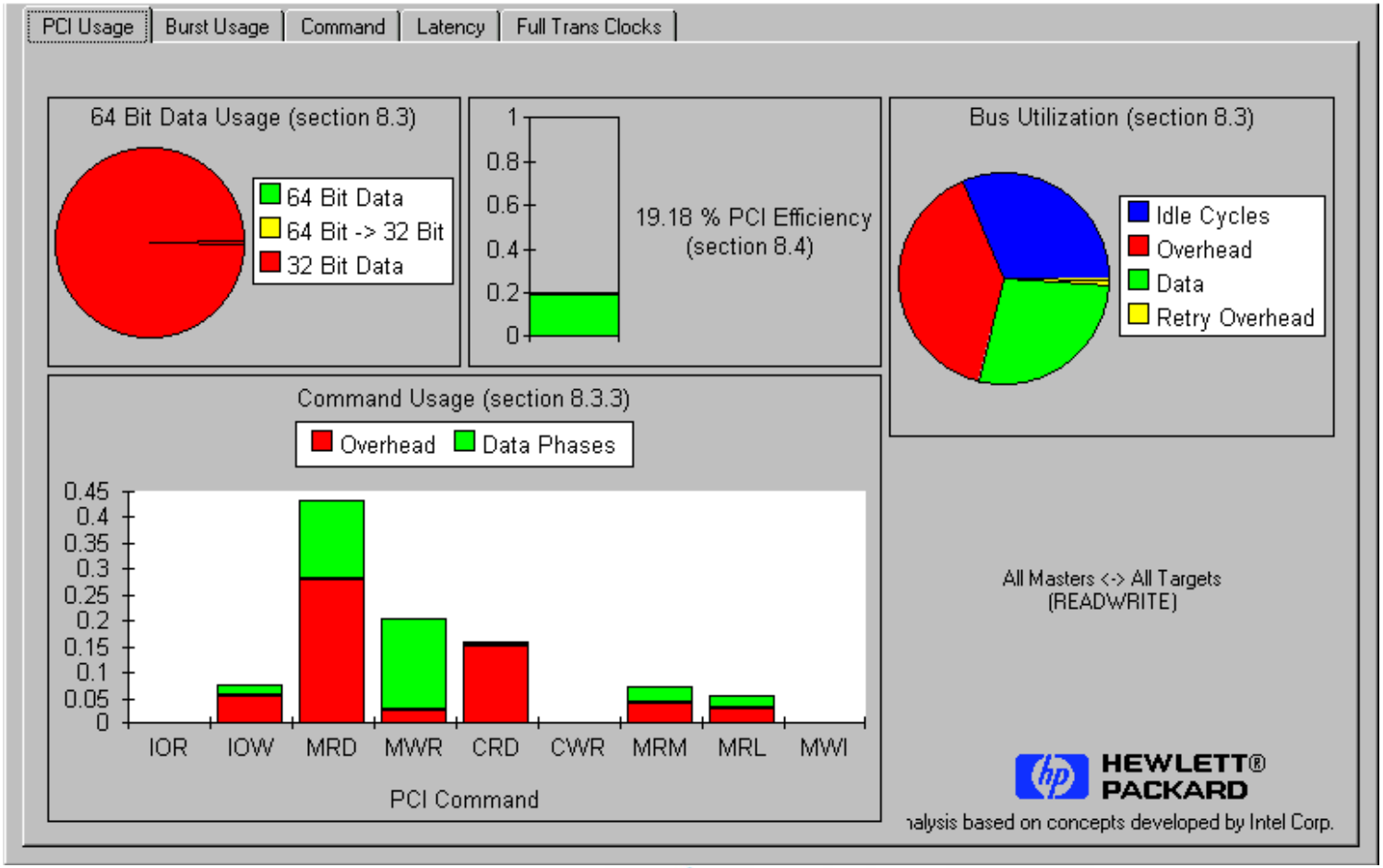
Performance Measurements: Utilization and Efficiency of Commands



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Performance Report (partial)

```
1.2 Statistical Base
--------------------
Test covered ......................     131512 clocks
Test covered ......................   0.00398521 sec
No of captured address cycles .....       6129 clocks
No of captured data cycles ........      37060 clocks
Number of Bytes transferred .......     138548 bytes
No of Interrupts occurred .........          0

2 BASIC BUS STATISTICS
======================
PCI Throughput ....................  34.7655 Megabytes/sec
                   .................. 278.1242 Megabits/sec
PCI Utilization ...................  68.67 %
Non-retry PCI Utilization .........  67.80 %
PCI Efficiency ....................  19.18 %
Non-retry PCI Efficiency ..........  19.42 %
```

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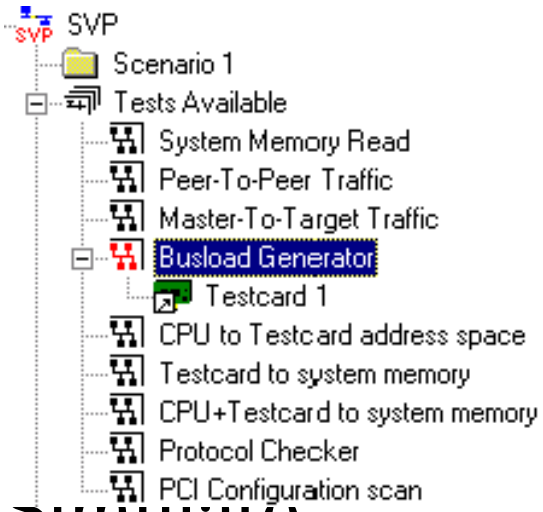
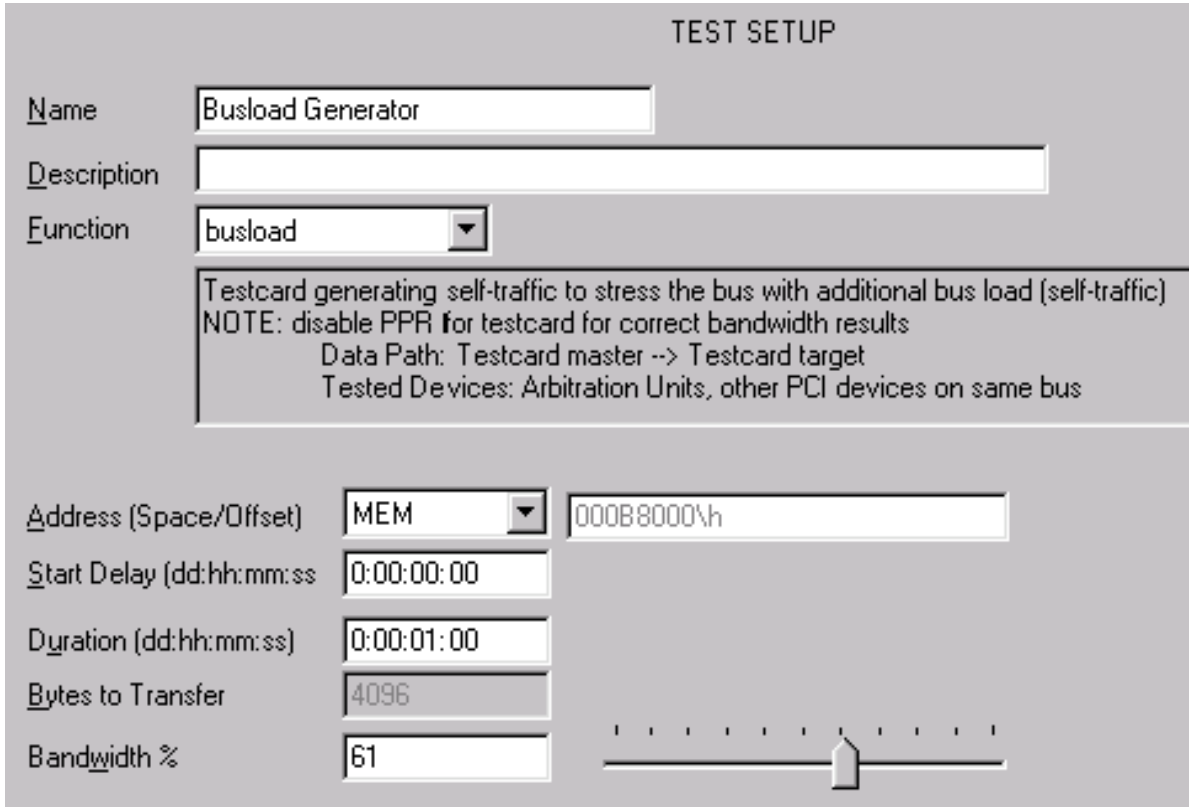
System Validation Package: Busload Generator





Simulate loaded system without having to populate with more cards.

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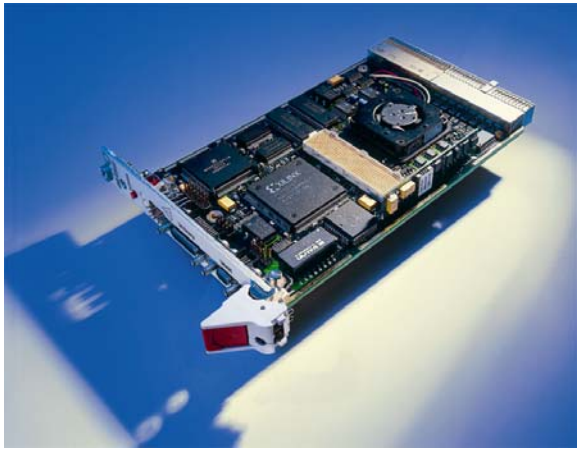
System Validation Package: Protocol Permutation and C-API

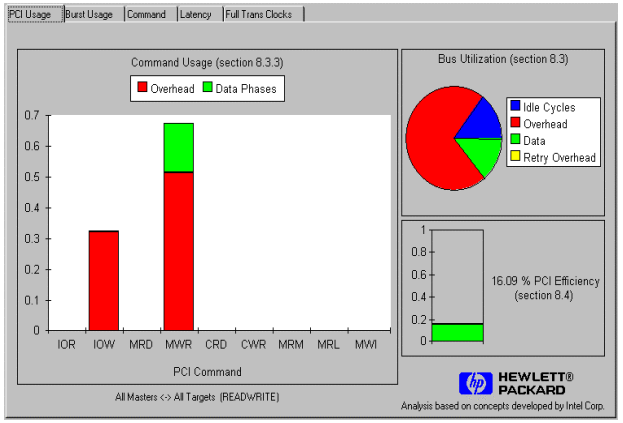
- Protocol Permutation and Randomization (PPR) allows more scenarios and corner cases to be checked in much less time with less programming and manual effort.
- Test parameters are permuted and randomized by PPR within limits set by the engineer.
- "Characterizing the performance of a PCI system typically took 2-3-4 days, almost a week. Now we can do it in as little as 15 minutes." Gregory McKnight, IBM Performance Lab.

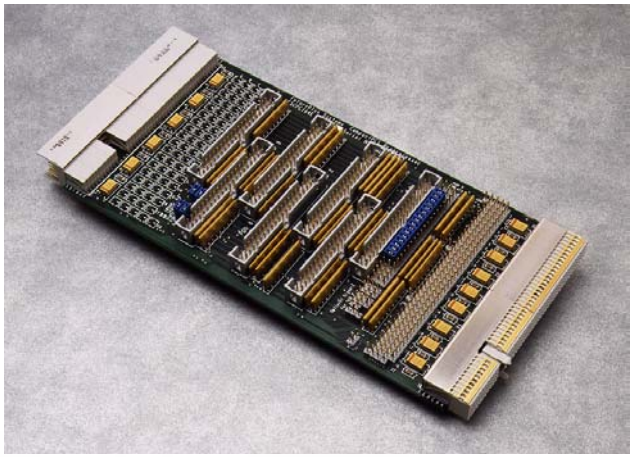
Conclusions

- CompactPCI systems require verification at the protocol, data and messaging levels.
- Active test equipment sitting on the PCI bus gives an excellent insight into the system under test.
- Use test equipment suited for the measurement.
- Agilent PCI Exerciser/Analyzers extend the classical debugging environment by adding predictable traffic generation capabilities.
- Agilent and FuturePlus test equipment supports the conversion from proprietary buses to CompactPCI.

Thank You!







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